REMARKS

The drawings were objected to as failing to comply with 37 CFR 1.84(p)(5) because they failed to include the reference sign 201. The reference sign 201 appears in the specification as the result of a typographical error. The specification has been amended to replace the reference sign 201 with 210 in both occurrences. In reviewing the drawings, however, it was discovered that the leader line from reference sign 100 extends to the wrong feature in FIG. 3. FIG. 3 has therefore been replaced with a corrected FIG. 3. A redline version of the drawing is included herewith to indicate the change.

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's FIG. 1 Prior Art in view of Ajika et al. (U.S. Patent No. 5,994,732). The Examiner states that it would have been obvious to one of ordinary skill in the art at the time of the invention to form memory cell transistors of each sector on a common bulk region as taught by Ajika et al., "for the purpose of preventing well disturbance in the erase operation."

Applicant respectfully traverses the Examiner's rejection. There is no teaching or motivation to combine Ajika et al. with Applicant's FIG. 1 prior art. One of ordinary skill in the art would not have combined Ajika et al. with Applicant's FIG. 1 prior art for the reasons stated by the Examiner. In particular, Ajika et al. teaches away from larger bulk regions in order to reduce the effects of erase operations in one erase block on adjacent erase blocks. *See, e.g.*, FIGS. 9 and 4; col. 2, line 62-col. 3, line 28. In particular, Ajika et al. explains that "[s]ome erase blocks 26 may be falsely erased when a large number of erase blocks are arranged within the same p well region 3*a*." Col. 3, lines 22-24.

Rather than extend the size and contents of the bulk region (e.g., p well), Ajika et al. teaches limiting the size and content of the p well *for the purpose of preventing well disturbance in the erase operation*. According to Ajika et al., "erase block 26 is preferably defined to include all of a plurality of memory transistors sharing one word line in one erase block 26. By limiting the size of an erase block to a single word line, the disturbance by the word line in the non-selected erase block can be effectively inhibited in the erase operation." Col. 7, line 65 – col. 8, line 2. The erase blocks are isolated from each other by forming an independent well for each erase block, "so that the well disturbance in the erase operation can be inhibited in a non-selected erase block." Col. 8, lines 7-11.

Applicant's invention, on the contrary, teaches enlargement of the bulk well. Applicant's invention is not directed toward preventing well disturbance in the erase operation. Furthermore, as can be seen in FIG. 4, the erase block of Applicant's invention

includes more than a single word line. There is accordingly no motivation or teaching to combine Ajika et al. with Applicant's FIG. 1 prior art.

For the foregoing reasons, reconsideration and allowance of claims 1-20 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

The paragraph beginning on page 4, line 13 has been rewritten as follows:

A column decoder block 102 is connected to the cell array block 101 to perform a decoding operation. The m number of bit lines are connected to each of the common data lines DLi through a corresponding column decoder. The common data lines include I number of lines DL0 to DLI-1. The common data lines are respectively connected to corresponding write drivers 200, [201] 210 and sense amplifiers 300, 310. All of the source terminals of the memory cell transistors in the cell array block 101 are connected to a common source line SL, driven by the source line driver 500. All of the memory cell transistors are further connected to a common bulk line Bulk at its bulk terminals. The common bulk line Bulk is driven by the bulk driver 400. The transistors T1, T2, T3 in the column decoder block 102 are formed in a separate bulk, which is grounded to 0 V.

The paragraph beginning on page 7, line 7 has been rewritten as follows:

In addition, a plurality of bit lines BL0 to BLm-1 are formed therein, where each of the bit lines BLi is commonly connected to m cell drains. The m bit lines are connected to each of the common data lines DLi through a corresponding column decoder. The common data lines include I lines DL0 to DLI-1. The common data lines are each respectively connected to a corresponding write driver 200, [201] 210 and sense amplifier 300, 310. The source terminals of the memory cell transistors in the cell block 101 are connected to one source line SL to thereby be driven by the source line driver 500.

FIG.3

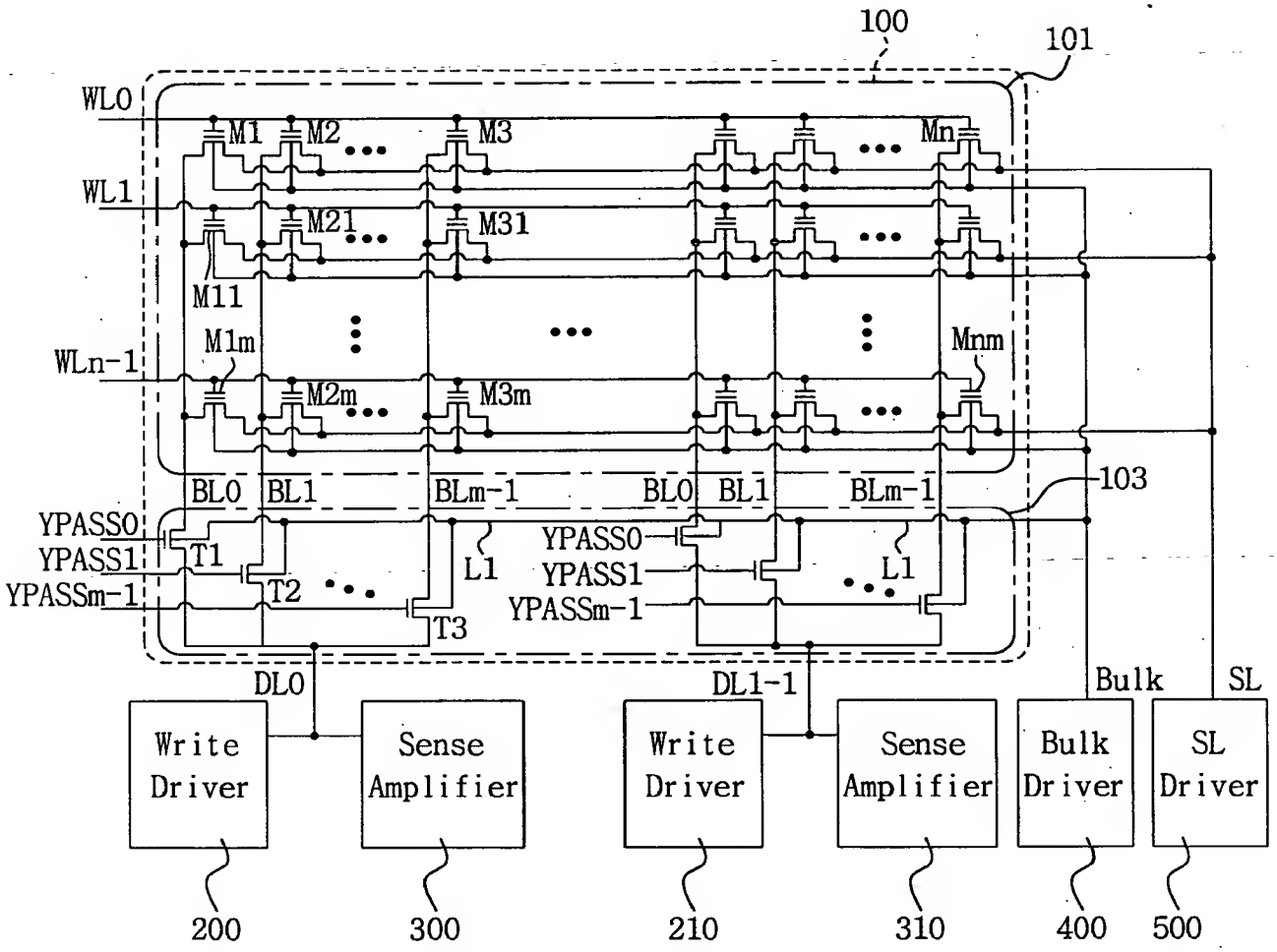
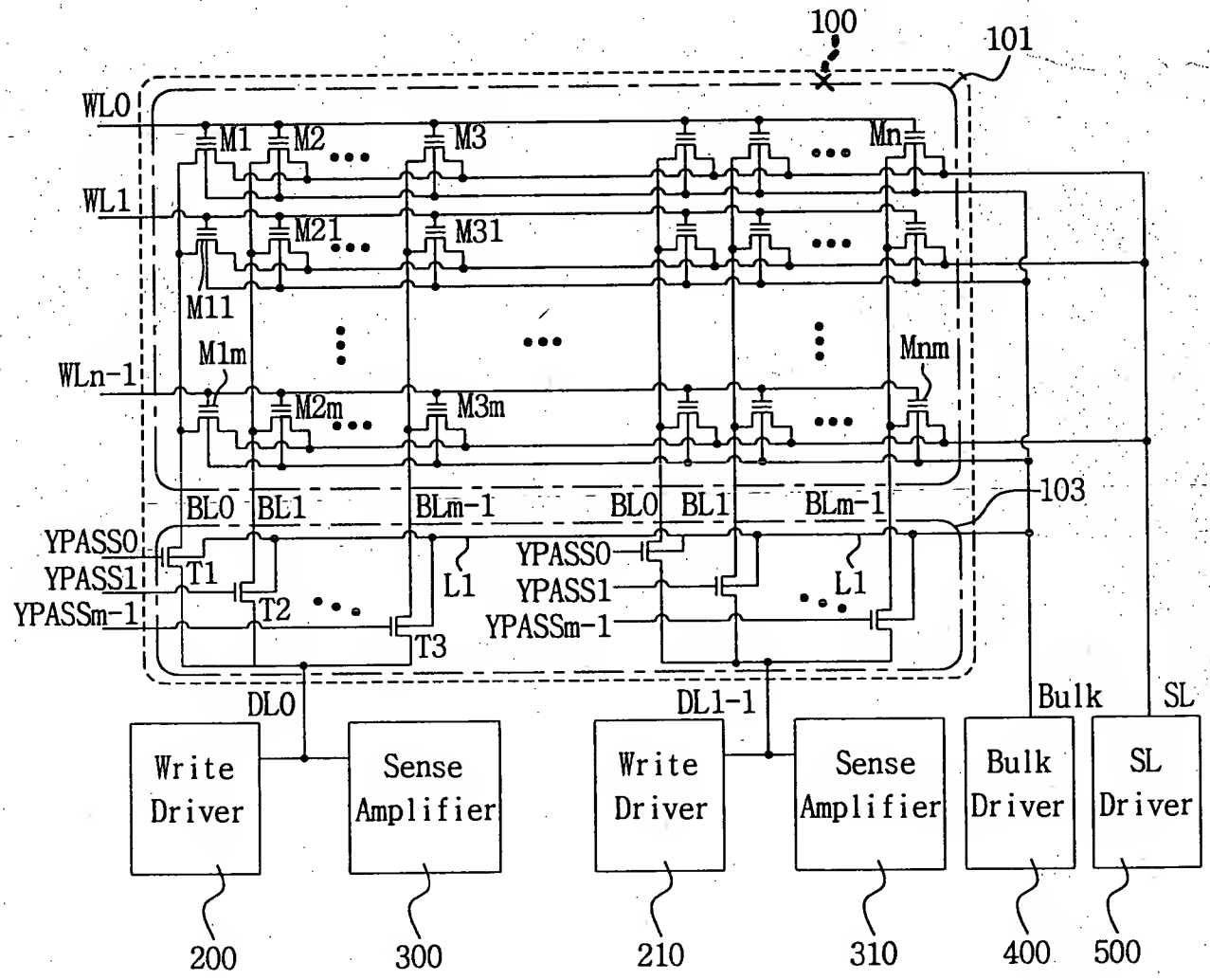


FIG.3



Approved
TP
11/12/02